Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A memory cell comprising:

a chalcogenide random access memory (CRAM) cell comprising a chalcogenide structure having a cross-sectional area, which is determined by a chalcogenide deposition thin film process and by an iso-etching process and which is relatively constant throughout a length of the chalcogenide structure; and

a CMOS circuit operative to access the CRAM cell.

2. (Original) The memory cell of claim 1, wherein the CRAM cell has cross-sectional area determined by a thin film process and by an iso-etching process.

3. (Cancelled)

4. (Original) The memory cell of claim 1, wherein the CRAM cell further comprises a chalcogenide structure in series with a semiconductor device.

5. (Original) The memory cell of claim 4, wherein the semiconductor device is a diode operative to drive a current through the chalcogenide structure.

6. (Original) The memory cell of claim 4, wherein the semiconductor device is a selecting transistor operative to drive a current through the chalcogenide structure when enabled by a voltage at a gate terminal of the selecting transistor.

7. (Original) The memory cell of claim 6, wherein:

the gate terminal of the selecting transistor is operatively coupled to a word line of a memory array;

a source terminal of the selecting transistor is operatively coupled to a drive line of the memory array; and

the drain terminal of the selecting transistor is operatively coupled to a bit line of the memory array.

8. (Currently Amended) A memory array comprising:

a plurality of chalcogenide random access memory (CRAM) cells, at least one of the CRAM cells comprising a chalcogenide structure having a cross-sectional area, which is determined by a thin film process and by an iso-etching process and which is relatively constant throughout a length of the chalcogenide structure;

a plurality of word lines each of which is operative to assert a data word, comprising a subset of the CRAM cells, in response to a CMOS circuit; and

a plurality of bit lines each of which is operative to access a CRAM cell of the plurality of CRAM cells, in response to an assertion of a word line.

9. (Currently Amended) The memory array of claim 8, wherein each of the CRAM cells of the plurality of CRAM cells has a chalcogenide structure having a cross-sectional area, which is determined by a thin film process and by an iso-etching process and which is relatively constant throughout a length of the chalcogenide structure.

10. (Currently Amended) The memory array of claim 9, wherein each of the CRAM cells of the plurality of CRAM cells has a chalcogenide structure having a cross-sectional area, which is determined by a chalcogenide deposition thin film process and by an iso-etching process and which is relatively constant throughout a length of the chalcogenide structure.

11. (Original) The memory array of claim 8, wherein each of the CRAM cells of the plurality of CRAM cells further comprises a chalcogenide structure in series with a semiconductor device.

12. (Original) The memory array of claim 11, wherein the semiconductor device is a diode operative to drive a current through the chalcogenide structure.

13. (Original) The memory array of claim 11, wherein the semiconductor device is a selecting transistor operative to drive a current through the chalcogenide structure when enabled by a voltage at a gate terminal of the selecting transistor.

14. (Original) The memory array of claim 13, wherein:

the gate terminal of the selecting transistor is operatively coupled to a word line of a memory array;

a source terminal of the selecting transistor is operatively coupled to a drive line of the memory array; and

the drain terminal of the selecting transistor is operatively coupled to a bit line of the memory array.

15-21. (Cancelled)